

# ABSTRACT

An object is to achieve reduction of a spurious in a delta-sigma type fraction division PLL synthesizer.

In its configuration, first and second L-value accumulators 31 and 30 are provided. The difference between overflow signals 16 and 17 of the first and the second L-value accumulators 31 and 30 is acquired by an adder 29, so that in response to an output signal of the adder 29, a division ratio of a variable divider 2 having a division ratio switchable between M, M+1, and M-1 is switched. By virtue of this, the frequency of a spurious generated by operation noise of the first and the second L-value accumulators 31 and 30 is shifted to a frequency component higher than the prior art so that the spurious is removed by a loop filter (low pass filter) 5.